ESP32-PICO-MINI-02
ESP32-PICO-MINI-02U

Datasheet Version 1.4

2.4 GHz Wi-Fi + Bluetooth® + Bluetooth LE module

Built around ESP32 series of SoCs, Xtensa® dual-core 32-bit LX6 microprocessor

Flash up to 8 MB, PSRAM up to 2 MB

27 GPIOs, rich set of peripherals

On-board PCB antenna or external antenna connector

ESP32-PICO-MINI-02

ESP32-PICO-MINI-02U

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1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/sites/default/files/documentation/esp32-pico-mini-02_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-PICO-V3-02 embedded, Xtensa dual-core 32-bit LX6 microprocessor, up to 240 MHz
- 448 KB ROM for booting and core functions
- 520 KB SRAM for data and instructions
- 16 KB SRAM in RTC
- 8 MB SPI flash
- 2 MB PSRAM

Wi-Fi

- 802.11b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Bluetooth®

- Bluetooth V4.2 BR/EDR and Bluetooth LE specification
- Class-1, class-2 and class-3 transmitter
- AFH
- CVSD and SBC

Peripherals

- Up to 27 GPIOs
  - 5 strapping GPIOs
  - 4 GPIOs used for in-package flash and PSRAM
  - 6 input-only GPIOs
- SD card, UART, SPI, SDIO, I2C, LED PWM, Motor PWM, I2S, IR, pulse counter, GPIO, capacitive touch sensor, ADC, DAC, TWAI® (compatible with ISO 11898-1, i.e. CAN Specification 2.0), Ethernet MAC

Integrated Components on Module

- 40 MHz crystal oscillator

Antenna Options

- ESP32-PICO-MINI-02: On-board PCB antenna
- ESP32-PICO-MINI-02U: external antenna via a connector

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: –40 ~ 85 °C

Certification

- RF certification: See certificates for ESP32-PICO-MINI-02 and ESP32-PICO-MINI-02U
- Green certification: REACH/RoHS

Test

- Reliability: HTOL/HTSL/uHAST/TCT/ESD

1.2 Series Comparison

ESP32-PICO-MINI-02 and ESP32-PICO-MINI-02U are two general-purpose Wi-Fi + Bluetooth + Bluetooth LE MCU modules. The rich set of peripherals and a small size make the two modules an ideal choice for a wide variety of IoT applications, ranging from home automation, smart building, consumer electronics to industrial control, and they are suitable for intelligent speakers, speech recognition toys, intelligent gateway and Ethernet, etc.

ESP32-PICO-MINI-02 comes with a PCB antenna. ESP32-PICO-MINI-02U comes with a connector for an external antenna.

They both feature an 8 MB in-package SPI flash and an additional 2 MB SPI Pseudo static RAM (PSRAM). The information in this datasheet is applicable to both modules.

The series comparison for the two modules is listed as follows:

Table 1: ESP32-PICO-MINI-02 Series Comparison[1]

Ordering Code	Flash	PSRAM	Ambient Temp.[2] (°C)	Size[3] (mm)
ESP32-PICO-MINI-02-N8R2	8 MB	2 MB	–40 ~ 85	13.2 × 16.6 × 2.4

[1] This table shares the same notes presented in Table 1 below.

Table 2: ESP32-PICO-MINI-02USeries Comparison

Ordering Code	Flash[4]	PSRAM	Ambient Temp.[2] (°C)	Size[3] (mm)
ESP32-PICO-MINI-02U-N8R2	8 MB	2 MB	–40 ~ 85	13.2 × 11.2 × 2.4

[2] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[3] For details, refer to Section 10.1 *Module Dimensions*.

[4] The flash is integrated in the chip's package. The flash supports:
- More than 100,000 program/erase cycles
- More than 20 years data retention time

At the core of the modules is the ESP32-PICO-V3-02 *. The chip embedded is designed to be scalable and adaptive. There are two CPU cores that can be individually controlled, and the CPU clock frequency is adjustable from 80 MHz to 240 MHz. You can power off the CPU and make use of the low-power coprocessor to constantly monitor the peripherals for changes or crossing of thresholds.

Note:
For more information on ESP32-PICO-V3-02, please refer to *ESP32-PICO Series Datasheet*.

1.3 Applications

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Speech Recognition
- Image Recognition
- SDIO Wi-Fi + Bluetooth Networking Card

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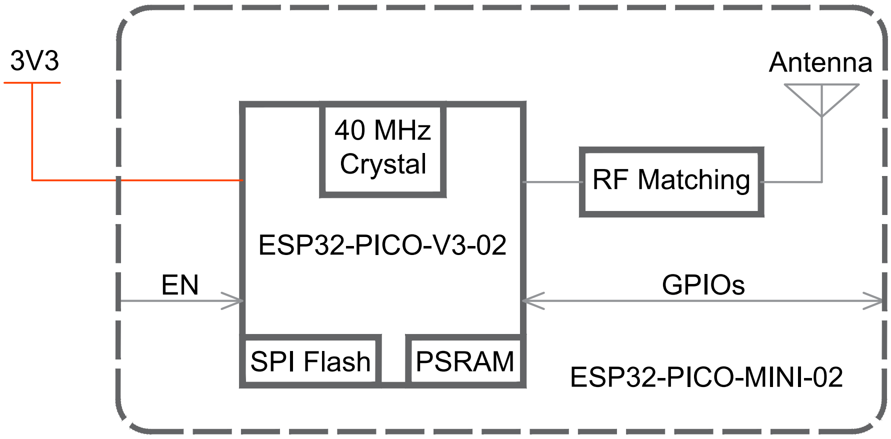

Figure 1: ESP32-PICO-MINI-02 Block Diagram

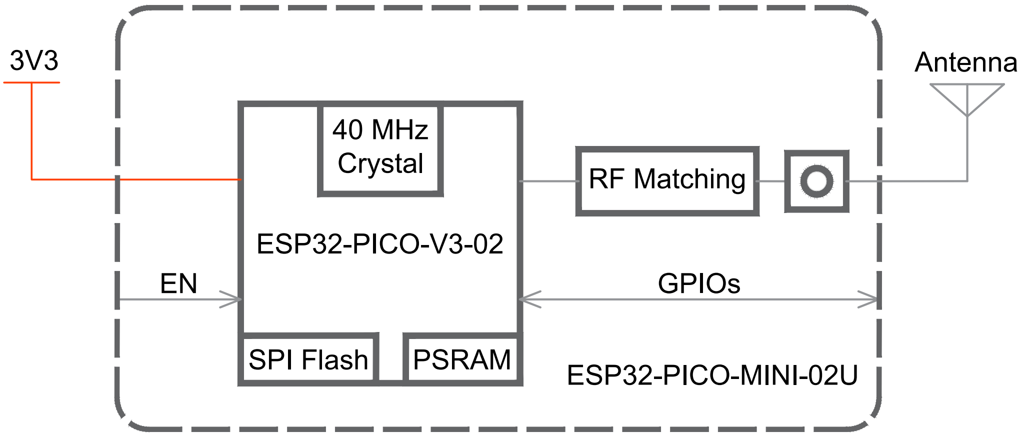

Figure 2: ESP32-PICO-MINI-02U Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 10.1 *Module Dimensions*.

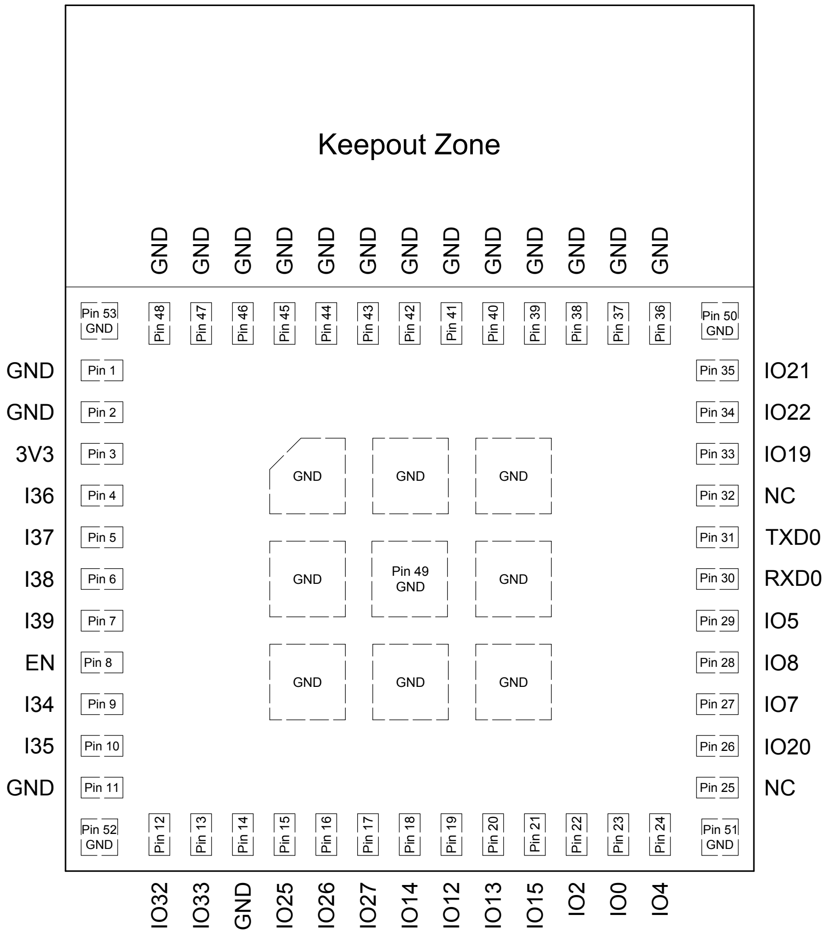

Figure 3: ESP32-PICO-MINI-02 Pin Layout (Top View)

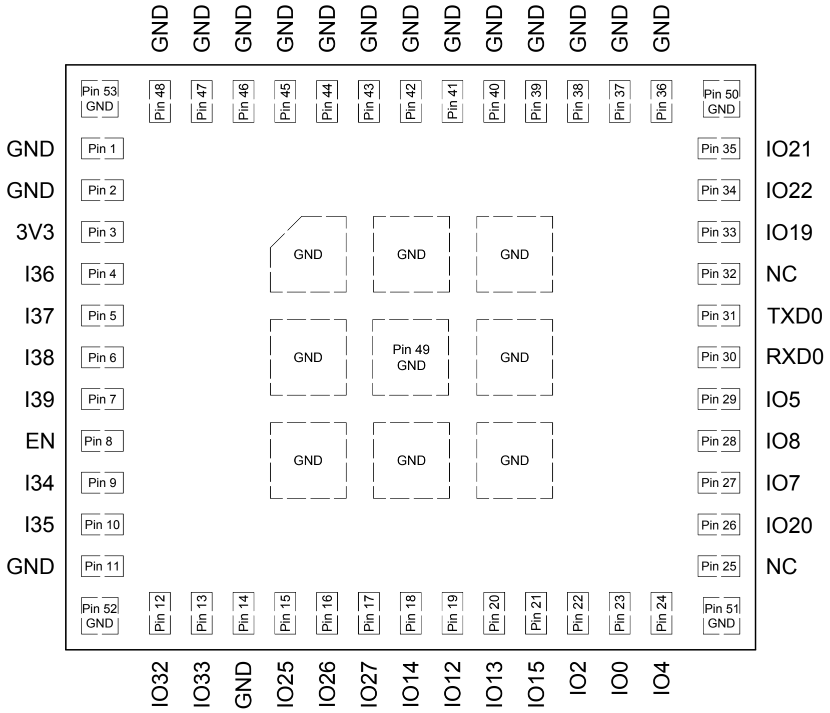

Figure 4: ESP32-PICO-MINI-02U Pin Layout (Top View)

3.2 Pin Description

ESP32-PICO-MINI-02 and ESP32-PICO-MINI-02U each has 53 pins. See pin definitions in Table 3 *Pin Description*.

For peripheral pin configurations, please refer to Section 5.2 *Digital Peripherals*.

Table 3: Pin Definitions

Name	No.	Type[1]	Function
GND	1, 2, 11, 14, 36-53	P	Ground
3V3	3	P	Power supply
I36	4	I	GPIO36, ADC1_CH0, RTC_GPIO0
I37	5	I	GPIO37, ADC1_CH1, RTC_GPIO1
I38	6	I	GPIO38, ADC1_CH2, RTC_GPIO2
I39	7	I	GPIO39, ADC1_CH3, RTC_GPIO3
EN	8	I	High: On; enables the chip Low: Off; the chip shuts down Note: Do not leave EN pin floating.
I34	9	I	GPIO34, ADC1_CH6, RTC_GPIO4
I35	10	I	GPIO35, ADC1_CH7, RTC_GPIO5
IO32	12	I/O	GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
IO33	13	I/O	GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8

Cont'd on next page

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Name	No.	Type[1]	Function
IO25	15	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	16	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	17	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
IO14	18	I/O	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
IO12	19	I/O	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
IO13	20	I/O	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
IO15	21	I/O	GPIO15, ADC2_CH3, TOUCH3, RTC_GPIO13, MTDO, HSPICS0, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	22	I/O	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	23	I/O	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	24	I/O	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
NC	25	-	-
IO20	26	I/O	GPIO20
IO7	27	I/O	GPIO7, HS1_DATA0, U2RTS, SD_DATA0
IO8	28	I/O	GPIO8, HS1_DATA1, U2CTS, SD_DATA1
IO5	29	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
RXD0	30	I/O	GPIO3, U0RXD, CLK_OUT2
TXD0	31	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
NC	32	-	-
IO19	33	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
IO22	34	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
IO21	35	I/O	GPIO21, VSPIHD, EMAC_TX_EN

* P: power supply; I: input; O: output.

* Pins CMD/IO11 and CLK/IO6 are used for connecting the embedded flash, and pins SD2/IO9 and SD3/IO10 are used for connecting embedded PSRAM. These pins are not led out.

4 Boot Configurations

Note:

The content below is excerpted from *ESP32 Series Datasheet* > Section *Boot Configurations*. For the strapping pin mapping between the chip and modules, please refer to Chapter 8 *Module Schematics*.

The chip allows for configuring the following boot parameters through strapping pins and eFuse bits at power-up or a hardware reset, without microcontroller interaction.

- Chip boot mode
  - Strapping pin: GPIO0 and GPIO2
- Internal LDO (VDD_SDIO) Voltage
  - Strapping pin: MTDI
  - eFuse bit: EFUSE_SDIO_FORCE and EFUSE_SDIO_TIEH
- U0TXD printing
  - Strapping pin: MTDO
- Timing of SDIO Slave
  - Strapping pin: MTDO and GPIO5
- JTAG signal source
  - eFuse bit: EFUSE_DISABLE_JTAG

The default values of all the above eFuse bits are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once an eFuse bit is programmed to 1, it can never be reverted to 0. For how to program eFuse bits, please refer to *ESP32 Technical Reference Manual* > Chapter *eFuse Controller*.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 4: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Pull-up	1
GPIO2	Pull-down	0
MTDI	Pull-down	0
MTDO	Pull-up	1
GPIO5	Pull-up	1

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 5 and Figure 5.

Table 5: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	1

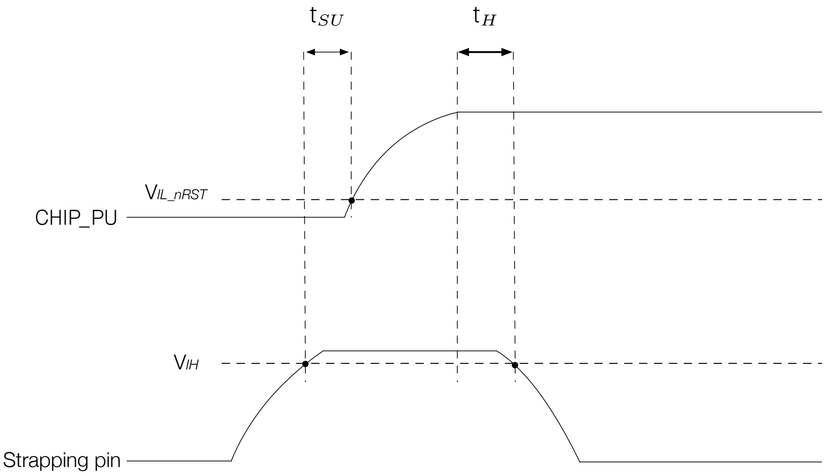

Figure 5: Visualization of Timing Parameters for the Strapping Pins

4.1 Chip Boot Mode Control

GPIO0 and GPIO2 control the boot mode after the reset is released. See Table 6 *Chip Boot Mode Control*.

Table 6: Chip Boot Mode Control

Boot Mode	GPIO0	GPIO2
SPI Boot Mode	**1**	Any value
Joint Download Boot Mode [2]	0	0

[1] **Bold** marks the default value and configuration.

[2] Joint Download Boot mode supports the following download methods:

- SDIO Download Boot
- UART Download Boot

In Joint Download Boot mode, the detailed boot flow of the chip is put below 6.

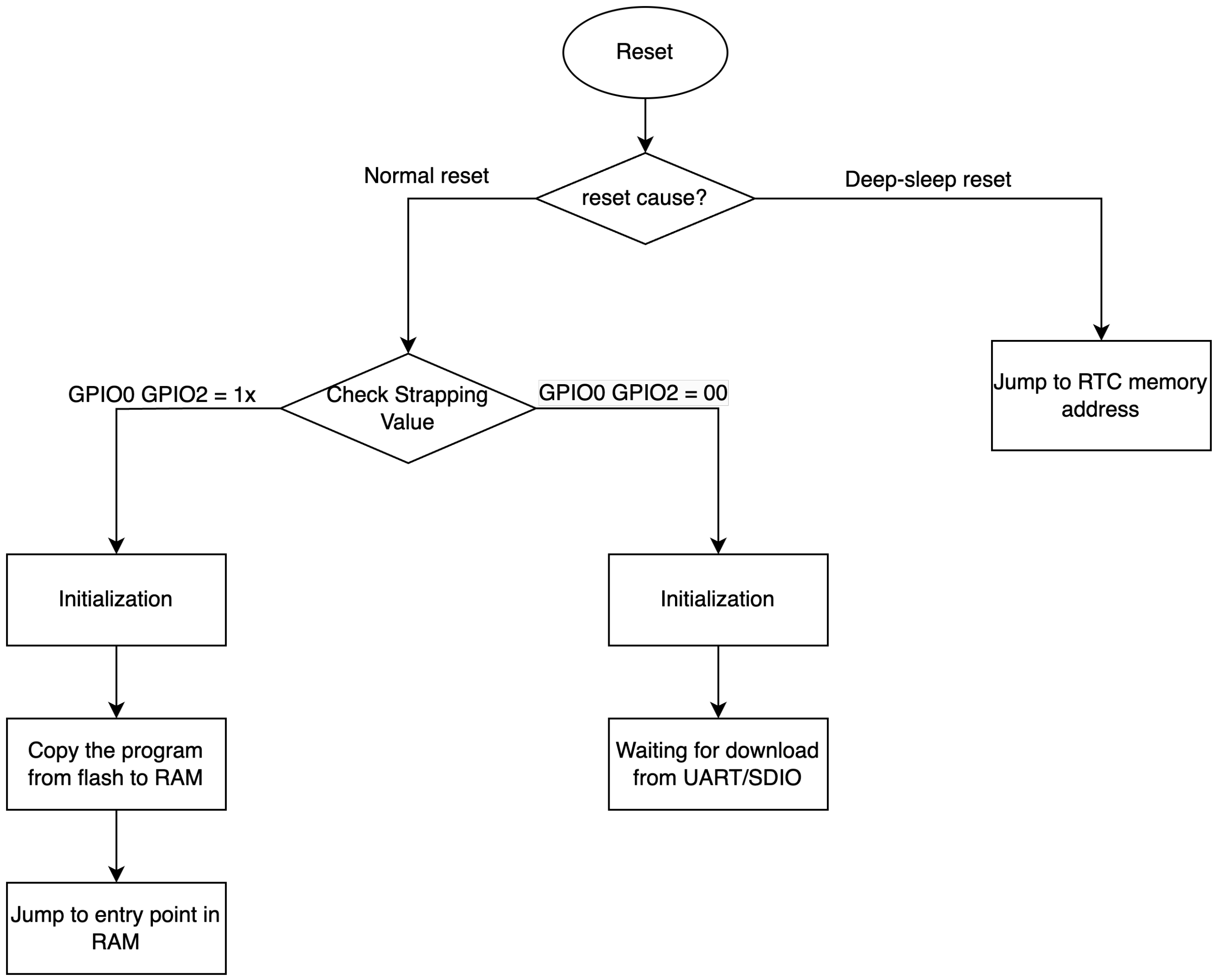

Figure 6: Chip Boot Flow

uart_download_dis controls boot mode behaviors:

It permanently disables Download Boot mode when uart_download_dis is set to 1 (valid only for ESP32 chip revisions v3.0 and higher).

4.2 Internal LDO (VDD_SDIO) Voltage Control

MTDI is used to select the VDD_SDIO power supply voltage at reset:

- MTDI = 0 (by default), VDD_SDIO pin is powered directly from VDD3P3_RTC. Typically this voltage is 3.3 V. For more information, see *ESP32 Series Datasheet* > Section *Power Scheme*.
- MTDI = 1, VDD_SDIO pin is powered from internal 1.8 V LDO.

This functionality can be overridden by setting EFUSE_SDIO_FORCE to 1, in which case the EFUSE_SDIO_TIEH determines the VDD_SDIO voltage:

- EFUSE_SDIO_TIEH = 0, VDD_SDIO connects to 1.8 V LDO.
- EFUSE_SPI_TIEH = 1, VDD_SDIO connects to VDD3P3_RTC.

4.3 U0TXD Printing Control

During booting, the strapping pin MTDO can be used to control the U0TXD Printing, as Table 7 shows.

Table 7: U0TXD Printing Control

U0TXD Printing Control	MTDO
Enabled [1]	**1**
Disabled	0

[1] **Bold** marks the default value and configuration.

4.4 Timing Control of SDIO Slave

The strapping pin MTDO and GPIO5 can be used to control the timing of SDIO slave, see Table 8 *Timing Control of SDIO Slave*.

Table 8: Timing Control of SDIO Slave

Edge behavior	MTDO	GPIO5
Falling edge sampling, falling edge output	0	0
Falling edge sampling, rising edge output	0	1
Rising edge sampling, falling edge output	1	0
Rising edge sampling, rising edge output	**1**	**1**

[1] **Bold** marks the default value and configuration.

4.5 JTAG Signal Source Control

If EFUSE_DISABLE_JTAG is set to 1, the source of JTAG signals can be disabled.

5 Peripherals

5.1 Peripheral Overview

ESP32-PICO-V3-02 chip integrates a rich set of peripherals including SPI, I2S, UART, I2C, pulse count controller, TWAI®, ADC, DAC, touch sensor, etc.

To learn more about on-chip components, please refer to ESP32 Series Datasheet > Section *Functional Description*.

Note:

- The content below is sourced from ESP32 Series Datasheet > Section *Functional Description*. Some information may not be applicable to ESP32-PICO-MINI-02 and ESP32-PICO-MINI-02U as not all the IO signals are exposed on the module.
- To learn more about peripheral signals, please refer to ESP32 Technical Reference Manual > Section *Peripheral Signal List*.

5.2 Digital Peripherals

5.2.1 General Purpose Input / Output Interface (GPIO)

ESP32 has 34 GPIO pins which can be assigned various functions by programming the appropriate registers. There are several kinds of GPIOs: digital-only, analog-enabled, capacitive-touch-enabled, etc. Analog-enabled GPIOs and Capacitive-touch-enabled GPIOs can be configured as digital GPIOs.

Most of the digital GPIOs can be configured as internal pull-up or pull-down, or set to high impedance. When configured as an input, the input value can be read through the register. The input can also be set to edge-trigger or level-trigger to generate CPU interrupts. Most of the digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the SDIO, UART, SPI, etc. (More details can be found in ESP32 Series Datasheet > Appendix, Table *IO_MUX*.) For low-power operations, the GPIOs can be set to hold their states.

5.2.2 Serial Peripheral Interface (SPI)

ESP32 integrates four SPI controllers which can be used to communicate with external devices that use the SPI protocol. Controller SPI0 is used as a buffer for accessing external memory. Controller SPI1 can be used as a master. Controllers SPI2 and SPI3 can be configured as either a master or a slave.

SPI1, SPI2, and SPI3 use signal buses prefixed with SPI, HSPI, and VSPI, respectively.

Features of General Purpose SPI (GP-SPI)

- Programmable data transfer length, in multiples of 1 byte
- Four-line full-duplex/half-duplex communication and three-line half-duplex communication support
- Master mode and slave mode

- Programmable CPOL and CPHA
- Programmable clock

Pin Assignment

For SPI, the pins are multiplexed with GPIO6 ~ GPIO11 via the IO MUX. For HSPI, the pins are multiplexed with GPIO2, GPIO4, GPIO12 ~ GPIO15 via the IO MUX. For VSPI, the pins are multiplexed with GPIO5, GPIO18 ~ GPIO19, GPIO21 ~ GPIO23 via the IO MUX.

For more information about the pin assignment, see *ESP32 Series Datasheet* > Section *Peripheral Pin Configurations* and *ESP32 Technical Reference Manual* > Chapter *IO_MUX and GPIO Matrix*.

5.2.3 Universal Asynchronous Receiver Transmitter (UART)

The UART in the ESP32 chip facilitates the transmission and reception of asynchronous serial data between the chip and external UART devices. It consists of two UARTs in the main system, and one low-power LP UART.

Feature List

- Programmable baud rate
- RAM shared by TX FIFOs and RX FIFOs
- Supports input baud rate self-check
- Support for various lengths of data bits and stop bits
- Parity bit support
- Asynchronous communication (RS232 and RS485) and IrDA support
- Supports DMA to communicate data in high speed
- Supports UART wake-up
- Supports both software and hardware flow control

Pin Assignment

The pins for UART can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32 Series Datasheet* > Section *Peripheral Pin Configurations* and *ESP32 Technical Reference Manual* > Chapter *IO_MUX and GPIO Matrix*.

5.2.4 I2C Interface

ESP32 has two I2C bus interfaces which can serve as I2C master or slave, depending on the user's configuration.

Feature List

- Two I2C controllers: one in the main system and one in the low-power system
- Standard mode (100 Kbit/s)

- Fast mode (400 Kbit/s)
- Up to 5 MHz, yet constrained by SDA pull-up strength
- Support for 7-bit and 10-bit addressing, as well as dual address mode
- Supports continuous data transmission with disabled Serial Clock Line (SCL)
- Supports programmable digital noise filter

Users can program command registers to control I2C interfaces, so that they have more flexibility.

Pin Assignment

For regular I2C, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see ESP32 Series Datasheet > Section *Peripheral Pin Configurations* and ESP32 Technical Reference Manual > Chapter *IO_MUX and GPIO Matrix*.

5.2.5 I2S Interface

The I2S Controller in the ESP32 chip provides a flexible communication interface for streaming digital data in multimedia applications, particularly digital audio applications.

Feature List

- Master mode and slave mode
- Full-duplex and half-duplex communications
- A variety of audio standards supported
- Configurable high-precision output clock
- Supports PDM signal input and output
- Configurable data transmit and receive modes

Pin Assignment

The pins for the I2S Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see ESP32 Series Datasheet > Section *Peripheral Pin Configurations* and ESP32 Technical Reference Manual > Chapter *IO_MUX and GPIO Matrix*.

5.2.6 Remote Control Peripheral

The Remote Control Peripheral (RMT) controls the transmission and reception of infrared remote control signals.

Feature List

- Eight channels for sending and receiving infrared remote control signals
- Independent transmission and reception capabilities for each channel
- Clock divider counter, state machine, and receiver for each RX channel

- Supports various infrared protocols

Pin Assignment

The pins for the Remote Control Peripheral can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see ESP32 Series Datasheet > Section *Peripheral Pin Configurations* and ESP32 Technical Reference Manual > Chapter *IO_MUX and GPIO Matrix*.

5.2.7 Pulse Counter Controller (PCNT)

The pulse counter controller (PCNT) is designed to count input pulses by tracking rising and falling edges of the input pulse signal.

Feature List

- Eight independent pulse counter units
- Each pulse counter unit has a 16-bit signed counter register and two channels
- Counter modes: increment, decrement, or disable
- Glitch filtering for input pulse signals and control signals
- Selection between counting on rising or falling edges of the input pulse signal

Pin Assignment

The pins for the Pulse Count Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see ESP32 Series Datasheet > Section *Peripheral Pin Configurations* and ESP32 Technical Reference Manual > Chapter *IO_MUX and GPIO Matrix*.

5.2.8 LED PWM Controller

The LED PWM Controller (LEDC) is designed to generate PWM signals for LED control.

Feature List

- Sixteen independent PWM generators
- Maximum PWM duty cycle resolution of 20 bits
- Eight independent timers with 20-bit counters, configurable fractional clock dividers and counter overflow values
- Adjustable phase of PWM signal output
- PWM duty cycle dithering
- Automatic duty cycle fading

Pin Assignment

The pins for the LED PWM Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32 Series Datasheet* > Section *Peripheral Pin Configurations* and *ESP32 Technical Reference Manual* > Chapter *IO_MUX and GPIO Matrix*.

5.2.9 Motor Control PWM

The Pulse Width Modulation (PWM) controller can be used for driving digital motors and smart lights. The controller consists of PWM timers, the PWM operator and a dedicated capture sub-module. Each timer provides timing in synchronous or independent form, and each PWM operator generates a waveform for one PWM channel. The dedicated capture sub-module can accurately capture events with external timing.

Feature List

- Three PWM timers for precise timing and frequency control
  - Every PWM timer has a dedicated 8-bit clock prescaler
  - The 16-bit counter in the PWM timer can work in count-up mode, count-down mode, or count-up-down mode
  - A hardware sync can trigger a reload on the PWM timer with a phase register. It will also trigger the prescaler' restart, so that the timer's clock can also be synced, with selectable hardware synchronization source
- Three PWM operators for generating waveform pairs
  - Six PWM outputs to operate in several topologies
  - Configurable dead time on rising and falling edges; each set up independently
  - Modulating of PWM output by high-frequency carrier signals, useful when gate drivers are insulated with a transformer
- Fault Detection module
  - Programmable fault handling in both cycle-by-cycle mode and one-shot mode
  - A fault condition can force the PWM output to either high or low logic levels
- Capture module for hardware-based signal processing
  - Speed measurement of rotating machinery
  - Measurement of elapsed time between position sensor pulses
  - Period and duty cycle measurement of pulse train signals
  - Decoding current or voltage amplitude derived from duty-cycle-encoded signals of current/voltage sensors
  - Three individual capture channels, each of which with a 32-bit time-stamp register
  - Selection of edge polarity and prescaling of input capture signals
  - The capture timer can sync with a PWM timer or external signals

Pin Assignment

The pins for the Motor Control PWM can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see ESP32 Series Datasheet > Section *Peripheral Pin Configurations* and ESP32 Technical Reference Manual > Chapter *IO_MUX and GPIO Matrix*.

5.2.10 SD/SDIO/MMC Host Controller

An SD/SDIO/MMC host controller is available on ESP32.

Feature List

- Supports two external cards
- Supports SD Memory Card standard: version 3.0 and version 3.01)
- Supports SDIO Version 3.0
- Supports Consumer Electronics Advanced Transport Architecture (CE-ATA Version 1.1)
- Supports Multimedia Cards (MMC version 4.41, eMMC version 4.5 and version 4.51)

The controller allows up to 80 MHz clock output in three different data-bus modes: 1-bit, 4-bit, and 8-bit modes. It supports two SD/SDIO/MMC4.41 cards in a 4-bit data-bus mode. It also supports one SD card operating at 1.8 V.

Pin Assignment

The pins for SD/SDIO/MMC Host Controller are multiplexed with GPIO2, GPIO4, GPIO6 ~ GPIO15 via IO MUX.

For more information about the pin assignment, see ESP32 Series Datasheet > Section *Peripheral Pin Configurations* and ESP32 Technical Reference Manual > Chapter *IO_MUX and GPIO Matrix*.

5.2.11 SDIO/SPI Slave Controller

ESP32 integrates an SD device interface that conforms to the industry-standard SDIO Card Specification Version 2.0, and allows a host controller to access the SoC, using the SDIO bus interface and protocol. ESP32 acts as the slave on the SDIO bus. The host can access the SDIO-interface registers directly and can access shared memory via a DMA engine, thus maximizing performance without engaging the processor cores.

Feature List

The SDIO/SPI slave controller supports the following features:

- SPI, 1-bit SDIO, and 4-bit SDIO transfer modes over the full clock range from 0 to 50 MHz
- Configurable sampling and driving clock edge
- Special registers for direct access by host
- Interrupts to host for initiating data transfer
- Automatic loading of SDIO bus data and automatic discarding of padding data
- Block size of up to 512 bytes
- Interrupt vectors between the host and the slave, allowing both to interrupt each other
- Supports DMA for data transfer

Pin Assignment

The pins for SDIO/SPI Slave Controller are multiplexed with GPIO2, GPIO4, GPIO6 ~ GPIO15 via IO MUX.

For more information about the pin assignment, see ESP32 Series Datasheet > Section *Peripheral Pin Configurations* and ESP32 Technical Reference Manual > Chapter *IO_MUX and GPIO Matrix*.

5.2.12 TWAI® Controller

The Two-wire Automotive Interface (TWAI®) is a multi-master, multi-cast communication protocol designed for automotive applications. The TWAI controller facilitates the communication based on this protocol.

Feature List

- Compatible with ISO 11898-1 protocol (CAN Specification 2.0)
- Standard frame format (11-bit ID) and extended frame format (29-bit ID)
- Bit rates:
  - From 25 Kbit/s to 1 Mbit/s in chip revision v0.0/v1.0/v1.1
  - From 12.5 Kbit/s to 1 Mbit/s in chip revision v3.0/v3.1
- Multiple modes of operation: Normal, Listen Only, and Self-Test
- 64-byte receive FIFO
- Special transmissions: single-shot transmissions and self reception
- Acceptance filter (single and dual filter modes)
- Error detection and handling: error counters, configurable error interrupt threshold, error code capture, arbitration lost capture

Pin Assignment

The pins for the Two-wire Automotive Interface can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see ESP32 Series Datasheet > Section *Peripheral Pin Configurations* and ESP32 Technical Reference Manual > Chapter *IO_MUX and GPIO Matrix*.

5.2.13 Ethernet MAC Interface

An IEEE-802.3-2008-compliant Media Access Controller (MAC) is provided for Ethernet LAN communications. ESP32 requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to ESP32 through 17 signals of MII or nine signals of RMII.

Feature List

- 10 Mbps and 100 Mbps rates
- Dedicated DMA controller allowing high-speed transfer between the dedicated SRAM and Ethernet MAC
- Tagged MAC frame (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation

- MAC control sublayer (control frames)
- 32-bit CRC generation and removal
- Several address-filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 512 words (32-bit)
- Hardware PTP (Precision Time Protocol) in accordance with IEEE 1588 2008 (PTP V2)
- 25 MHz/50 MHz clock output

Pin Assignment

For information about the pin assignment of Ethernet MAC Interface, see *ESP32 Series Datasheet* > Section *Peripheral Pin Configurations* and *ESP32 Technical Reference Manual* > Chapter *IO_MUX and GPIO Matrix*.

5.3 Analog Peripherals

5.3.1 Analog-to-Digital Converter (ADC)

ESP32 integrates two 12-bit SAR ADCs and supports measurements on 18 channels (analog-enabled pins). The ULP coprocessor in ESP32 is also designed to measure voltage, while operating in the sleep mode, which enables low-power consumption. The CPU can be woken up by a threshold setting and/or via other triggers.

Table 9 describes the ADC characteristics.

Table 9: ADC Characteristics

Parameter	Description	Min	Max	Unit
DNL (Differential nonlinearity)	RTC controller; ADC connected to an external 100 nF capacitor; DC signal input; ambient temperature at 25 °C; Wi-Fi&Bluetooth off	–7	7	LSB
INL (Integral nonlinearity)		–12	12	LSB
Sampling rate	RTC controller	—	200	ksps
	DIG controller	—	2	Msps

Notes:

- When atten = 3 and the measurement result is above 3000 (voltage at approx. 2450 mV), the ADC accuracy will be worse than described in the table above.
- To get better DNL results, users can take multiple sampling tests with a filter, or calculate the average value.
- The input voltage range of GPIO pins within VDD3P3_RTC domain should strictly follow the DC characteristics provided in Table 14. Otherwise, measurement errors may be introduced, and chip performance may be affected.

By default, there are ±6% differences in measured results between chips. ESP-IDF provides couple of calibration methods for ADC1. Results after calibration using eFuse Vref value are shown in Table 10. For higher accuracy, users may apply other calibration methods provided in ESP-IDF, or implement their own.

Table 10: ADC Calibration Results

Parameter	Description	Min	Max	Unit
Total error	Atten = 0, effective measurement range of 100 ~ 950 mV	–23	23	mV
	Atten = 1, effective measurement range of 100 ~ 1250 mV	–30	30	mV
	Atten = 2, effective measurement range of 150 ~ 1750 mV	–40	40	mV
	Atten = 3, effective measurement range of 150 ~ 2450 mV	–60	60	mV

Pin Assignment

With appropriate settings, the ADCs can be configured to measure voltage on 18 pins maximum. For detailed information about the pin assignment, see *ESP32 Series Datasheet* > Section *Peripheral Pin Configurations* and *ESP32 Technical Reference Manual* > Chapter *IO_MUX and GPIO Matrix*.

5.3.2 Digital-to-Analog Converter (DAC)

Two 8-bit DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and a buffer. This dual DAC supports power supply as input voltage reference. The two DAC channels can also support independent conversions.

Pin Assignment

The DAC can be configured by GPIO 25 and GPIO 26. For detailed information about the pin assignment, see *ESP32 Series Datasheet* > Section *Peripheral Pin Configurations* and *ESP32 Technical Reference Manual* > Chapter *IO_MUX and GPIO Matrix*.

5.3.3 Touch Sensor

ESP32 has 10 capacitive-sensing GPIOs, which detect variations induced by touching or approaching the GPIOs with a finger or other objects. The low-noise nature of the design and the high sensitivity of the circuit allow relatively small pads to be used. Arrays of pads can also be used, so that a larger area or more points can be detected.

Pin Assignment

The 10 capacitive-sensing GPIOs are listed in Table 11.

Table 11: Capacitive-Sensing GPIOs Available on ESP32

Capacitive-Sensing Signal Name	Pin Name
T0	GPIO4
T1	GPIO0
T2	GPIO2
T3	MTDO
T4	MTCK

Capacitive-Sensing Signal Name	Pin Name
T5	MTDI
T6	MTMS
T7	GPIO27
T8	32K_XN
T9	32K_XP

Note:
ESP32 Touch Sensor has not passed the Conducted Susceptibility (CS) test for now, and thus has limited application scenarios.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses above those listed in Table 12 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in Section 13 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 12: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	85	°C

[*] For IO's power domain, please see *ESP32 Series Datasheet* > Appendix *IO MUX*.

6.2 Recommended Operating Conditions

Table 13: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T	Operating ambient temperature	–40	—	85	°C

6.3 DC Characteristics (3.3 V, 25 °C)

Table 14: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}	Low-level output voltage	—	—	0.1 × VDD[1]	V

Cont'd on next page

Table 14 – cont'd from previous page

Symbol	Parameter		Min	Typ	Max	Unit
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain [1, 2]	—	40	—	mA
		VDD3P3_RTC power domain [1, 2]	—	40	—	mA
		VDD_SDIO power domain [1, 3]	—	20	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)		—	28	—	mA
R_{PU}	Resistance of internal pull-up resistor		—	45	—	kΩ
R_{PD}	Resistance of internal pull-down resistor		—	45	—	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to shut down the chip		—	—	0.6	V

[1] Please see Appendix IO MUX of *ESP32 Series Datasheet* for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.

[2] For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, V_{OH}>=2.64 V, as the number of current-source pins increases.

[3] Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

6.4 Current Consumption Characteristics

6.4.1 Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 15: Current Consumption Depending on RF Modes

Work mode	Description		Peak (mA)
Active (RF working)	TX	802.11b, 20 MHz, 1 Mbps, @19.5 dBm	368
		802.11g, 20 MHz, 54 Mbps, @14 dBm	258
		802.11n, 20 MHz, MCS7, @13 dBm	248
		802.11n, 40 MHz, MCS7, @13 dBm	250
	RX	802.11b/g/n, 20 MHz	111
		802.11n, 40 MHz	117

6.4.2 Current Consumption in Other Modes

Table 16: Current Consumption Depending on Work Modes

Work mode	Description		Current consumption (Typ)
Modem-sleep [1, 2]	The CPU is powered on [3]	240 MHz	30 ~ 68 mA
		160 MHz	27 ~ 44 mA
		Normal speed: 80 MHz	20 ~ 31 mA
Light-sleep	—		0.8 mA
Deep-sleep	The ULP coprocessor is powered up [4]		150 μA
	ULP sensor-monitored pattern [5]		100 μA @1% duty
	RTC timer + RTC memory		10 μA
	RTC timer only		5 μA
Power off	CHIP_PU is set to low level, the chip is powered down		1 μA

[1] The current consumption figures in Modem-sleep mode are for cases where the CPU is powered up and the cache idle.

[2] When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, current consumption changes accordingly.

[3] In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.

[4] During Deep-sleep, when the ULP coprocessor is powered up, peripherals such as GPIO and RTC I2C are able to operate.

[5] The ”ULP sensor-monitored pattern” refers to the mode where the ULP coprocessor or the sensor works periodically. When ADC works with a duty cycle of 1%, the typical current consumption is 100 μA.

7 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The external antennas used for the tests on the modules with external antenna connectors have an impedance of 50 Ω.Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

7.1 Wi-Fi Radio

Table 17: Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n

7.1.1 Wi-Fi RF Transmitter (TX) Characteristics

Table 18: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	19.5	—
802.11b, 11 Mbps	—	19.5	—
802.11g, 6 Mbps	—	18.0	—
802.11g, 54 Mbps	—	14.0	—
802.11n, HT20, MCS0	—	18.0	—
802.11n, HT20, MCS7	—	13.0	—
802.11n, HT40, MCS0	—	18.0	—
802.11n, HT40, MCS7	—	13.0	—

Table 19: TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, DSSS	—	–26.5	–10.0
802.11b, 11 Mbps, CCK	—	–26.5	–10.0
802.11g, 6 Mbps, OFDM	—	–24.0	–5.0
802.11g, 54 Mbps, OFDM	—	–30.0	–25.0
802.11n, HT20, MCS0	—	–24.0	–5.0

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Table 19 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11n, HT20, MCS7	—	–30.5	–27.0
802.11n, HT40, MCS0	—	–24.0	–5.0
802.11n, HT40, MCS7	—	–30.5	–27.0

[1] EVM is measured at the corresponding typical TX power provided in Table *18 Wi-Fi RF Transmitter (TX) Characteristics* above.

7.1.2 Wi-Fi RF Receiver (RX) Characteristics

Table 20: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	–97.0	—
802.11b, 2 Mbps, DSSS	—	–94.0	—
802.11b, 5.5 Mbps, CCK	—	–92.0	—
802.11b, 11 Mbps, CCK	—	–88.0	—
802.11g, 6 Mbps, OFDM	—	–93.0	—
802.11g, 9 Mbps, OFDM	—	–91.0	—
802.11g, 12 Mbps, OFDM	—	–89.0	—
802.11g, 18 Mbps, OFDM	—	–87.0	—
802.11g, 24 Mbps, OFDM	—	–84.0	—
802.11g, 36 Mbps, OFDM	—	–80.0	—
802.11g, 48 Mbps, OFDM	—	–77.0	—
802.11g, 54 Mbps, OFDM	—	–75.0	—
802.11n, HT20, MCS0	—	–92.0	—
802.11n, HT20, MCS1	—	–88.0	—
802.11n, HT20, MCS2	—	–86.0	—
802.11n, HT20, MCS3	—	–83.0	—
802.11n, HT20, MCS4	—	–80.0	—
802.11n, HT20, MCS5	—	–76.0	—
802.11n, HT20, MCS6	—	–74.0	—
802.11n, HT20, MCS7	—	–72.0	—
802.11n, HT40, MCS0	—	–89.0	—
802.11n, HT40, MCS1	—	–85.0	—
802.11n, HT40, MCS2	—	–83.0	—
802.11n, HT40, MCS3	—	–80.0	—
802.11n, HT40, MCS4	—	–76.0	—
802.11n, HT40, MCS5	—	–72.0	—
802.11n, HT40, MCS6	—	–71.0	—
802.11n, HT40, MCS7	—	–69.0	—

Table 21: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	0	—
802.11g, 54 Mbps	—	–8	—
802.11n, HT20, MCS0	—	0	—
802.11n, HT20, MCS7	—	–8	—
802.11n, HT40, MCS0	—	0	—
802.11n, HT40, MCS7	—	–8	—

Table 22: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps, DSSS	—	35	—
802.11b, 11 Mbps, CCK	—	35	—
802.11g, 6 Mbps, OFDM	—	27	—
802.11g, 54 Mbps, OFDM	—	13	—
802.11n, HT20, MCS0	—	27	—
802.11n, HT20, MCS7	—	12	—
802.11n, HT40, MCS0	—	16	—
802.11n, HT40, MCS7	—	7	—

7.2 Bluetooth Radio

7.2.1 Transmitter – Basic Data Rate

Table 23: Transmitter Characteristics – Basic Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power*	-	-	0	-	dBm
Gain control step	-	-	3	-	dB
RF power control range	-	–12	-	+9	dBm
+20 dB bandwidth	-	-	0.9	-	MHz
Adjacent channel transmit power	F = F0 ± 2 MHz	-	–55	-	dBm
	F = F0 ± 3 MHz	-	–55	-	dBm
	F = F0 ± > 3 MHz	-	–59	-	dBm
$\Delta f1_{\text{avg}}$	-	-	-	155	kHz
$\Delta f2_{\text{max}}$	-	127	-	-	kHz
$\Delta f2_{\text{avg}}/\Delta f1_{\text{avg}}$	-	-	0.92	-	-
ICFT	-	-	–7	-	kHz

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Table 23 – cont'd from previous page

Parameter	Conditions	Min	Typ	Max	Unit
Drift rate	-	-	0.7	-	kHz/50 μs
Drift (DH1)	-	-	6	-	kHz
Drift (DH5)	-	-	6	-	kHz

* There are a total of eight power levels from 0 to 7, and the transmit power ranges from –12 dBm to 9 dBm. When the power level rises by 1, the transmit power increases by 3 dB. Power level 4 is used by default and the corresponding transmit power is 0 dBm.

7.2.2 Receiver – Basic Data Rate

Table 24: Receiver Characteristics – Basic Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @0.1% BER	—	–90	–89	–88	dBm
Maximum received signal @0.1% BER	—	0	—	—	dBm
Co-channel C/I	—	—	+7	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	—	–6	dB
	F = F0 – 1 MHz	—	—	–6	dB
	F = F0 + 2 MHz	—	—	–25	dB
	F = F0 – 2 MHz	—	—	–33	dB
	F = F0 + 3 MHz	—	—	–25	dB
	F = F0 – 3 MHz	—	—	–45	dB

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Table 24 – cont'd from previous page

Parameter	Conditions	Min	Typ	Max	Unit
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	—	—	dBm
	2000 MHz ~ 2400 MHz	–27	—	—	dBm
	2500 MHz ~ 3000 MHz	–27	—	—	dBm
	3000 MHz ~ 12.5 GHz	–10	—	—	dBm
Intermodulation	—	–36	—	—	dBm

7.2.3 Transmitter – Enhanced Data Rate

Table 25: Transmitter Characteristics – Enhanced Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power (see note under Table 23)	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
$\pi/4$ DQPSK max w0	—	—	–0.72	—	kHz
$\pi/4$ DQPSK max wi	—	—	–6	—	kHz
$\pi/4$ DQPSK max $\|$wi + w0$\|$	—	—	–7.42	—	kHz
8DPSK max w0	—	—	0.7	—	kHz
8DPSK max wi	—	—	–9.6	—	kHz
8DPSK max $\|$wi + w0$\|$	—	—	–10	—	kHz
$\pi/4$ DQPSK modulation accuracy	RMS DEVM	—	4.28	—	%
	99% DEVM	—	100	—	%
	Peak DEVM	—	13.3	—	%
8 DPSK modulation accuracy	RMS DEVM	—	5.8	—	%
	99% DEVM	—	100	—	%
	Peak DEVM	—	14	—	%
In-band spurious emissions	F = F0 ± 1 MHz	—	–46	—	dBm
	F = F0 ± 2 MHz	—	–44	—	dBm
	F = F0 ± 3 MHz	—	–49	—	dBm
	F = F0 +/– > 3 MHz	—	—	–53	dBm
EDR differential phase coding	—	—	100	—	%

7.2.4 Receiver – Enhanced Data Rate

Table 26: Receiver Characteristics – Enhanced Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
$\pi/4$ DQPSK					
Sensitivity @0.01% BER	—	–90	–89	–88	dBm
Maximum received signal @0.01% BER	—	—	0	—	dBm
Co-channel C/I	—	—	11	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–7	—	dB

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Table 26 – cont'd from previous page

Parameter	Conditions	Min	Typ	Max	Unit
	F = F0 – 1 MHz	—	–7	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–35	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–45	—	dB
8DPSK					
Sensitivity @0.01% BER	—	–84	–83	–82	dBm
Maximum received signal @0.01% BER	—	—	–5	—	dBm
C/I c-channel	—	—	18	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	2	—	dB
	F = F0 – 1 MHz	—	2	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–25	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–38	—	dB

7.3 Bluetooth LE Radio

Table 27: Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	–12.0 ~ 9.0 dBm

7.3.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 28: Transmitter Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power (see note under Table 23)	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
Adjacent channel transmit power	F = F0 ± 2 MHz	—	–52	—	dBm
	F = F0 ± 3 MHz	—	–58	—	dBm
	F = F0 ± > 3 MHz	—	–60	—	dBm
$\Delta f1_{\text{avg}}$	—	—	—	265	kHz
$\Delta f2_{\text{max}}$	—	247	—	—	kHz
$\Delta f2_{\text{avg}}/\Delta f1_{\text{avg}}$	—	—	+0.92	—	—
ICFT	—	—	–10	—	kHz
Drift rate	—	—	0.7	—	kHz/50 μs
Drift	—	—	2	—	kHz

7.3.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 29: Receiver Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	–94	–93	–92	dBm
Maximum received signal @30.8% PER	—	0	—	—	dBm
Co-channel C/I	—	—	+10	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–5	—	dB
	F = F0 – 1 MHz	—	–5	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–35	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–45	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	—	—	dBm
	2000 MHz ~ 2400 MHz	–27	—	—	dBm
	2500 MHz ~ 3000 MHz	–27	—	—	dBm
	3000 MHz ~ 12.5 GHz	–10	—	—	dBm
Intermodulation	—	–36	—	—	dBm

8 Module Schematics

This is the reference design of the module.

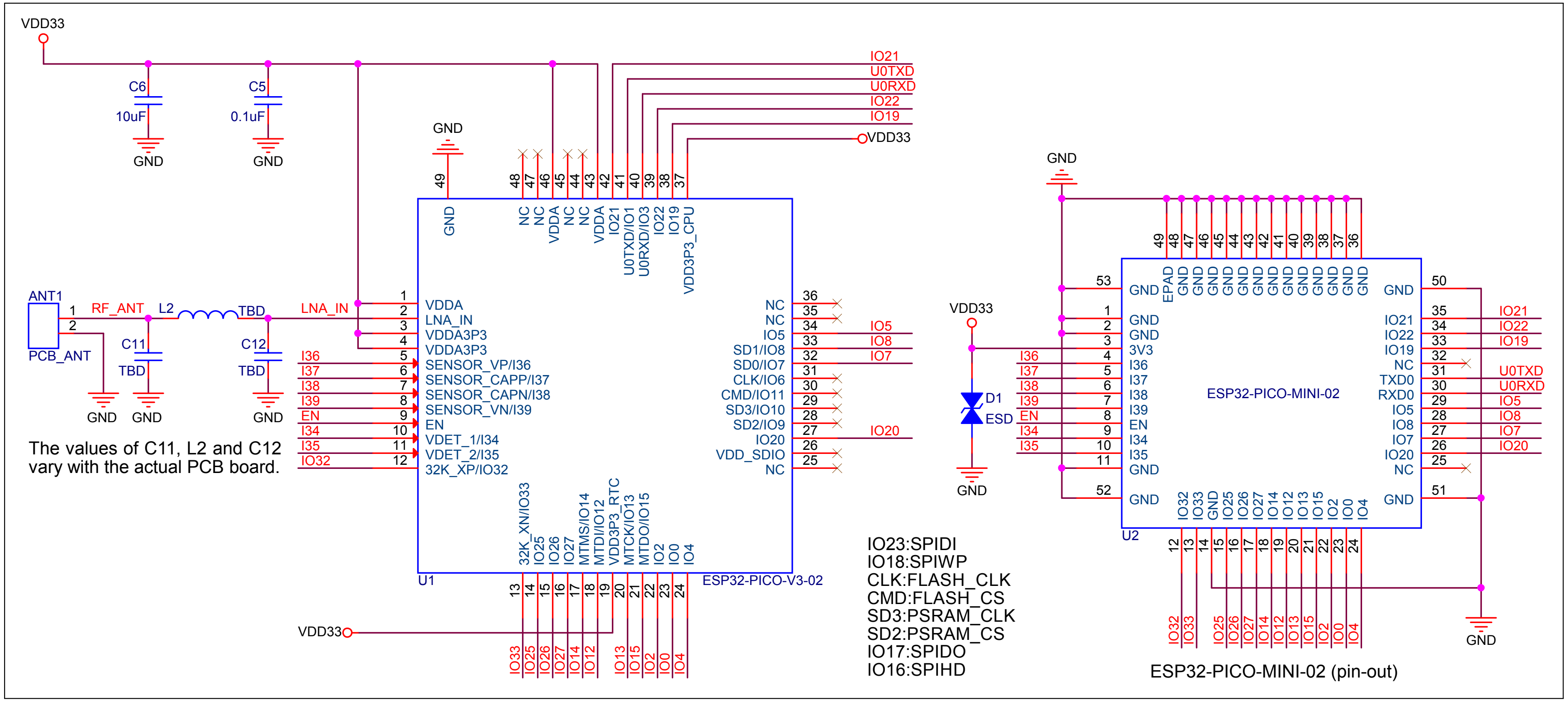
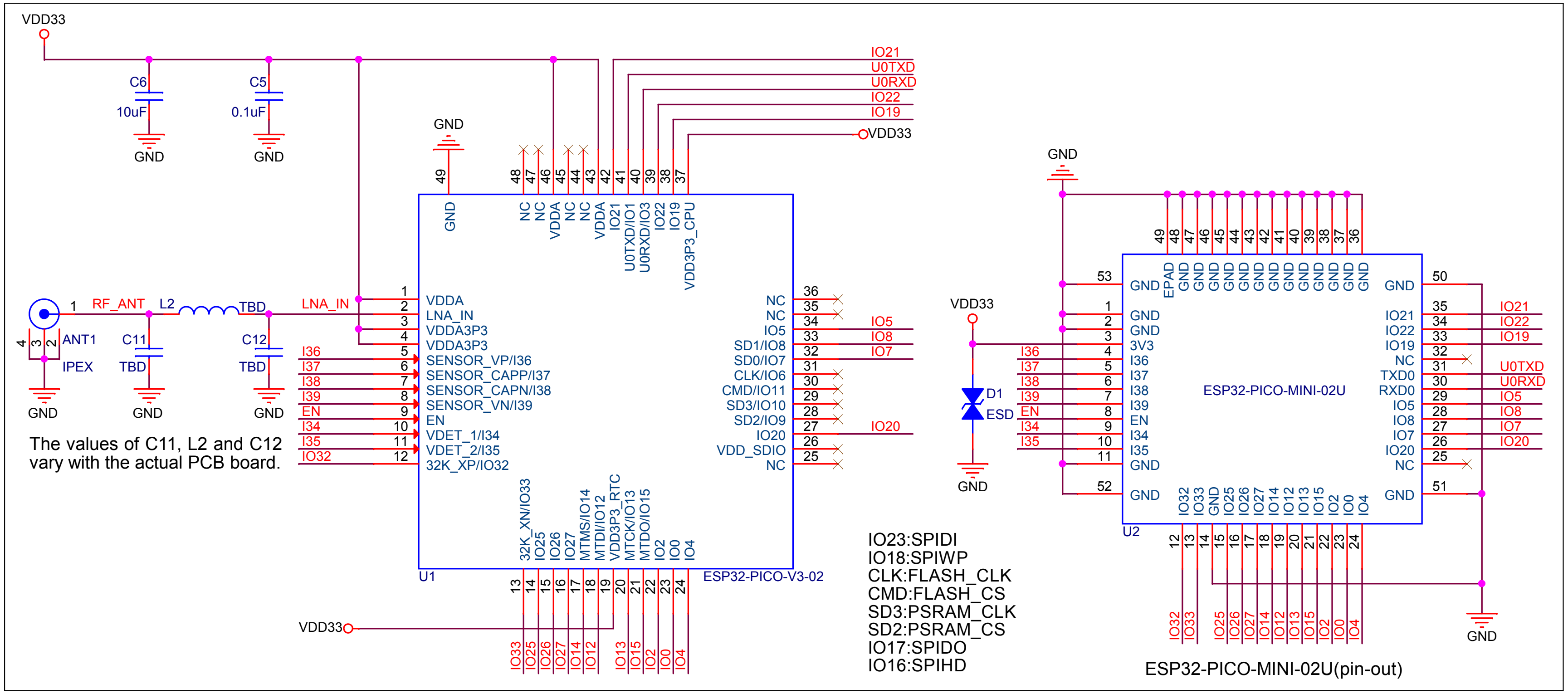


Figure 7: ESP32-PICO-MINI-02 Schematics



The values of C11, L2 and C12 vary with the actual PCB board.

IO23:SPIDI
IO18:SPIWP
CLK:FLASH_CLK
CMD:FLASH_CS
SD3:PSRAM_CLK
SD2:PSRAM_CS
IO17:SPIDO
IO16:SPIHD

Figure 8: ESP32-PICO-MINI-02U Schematics

9 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

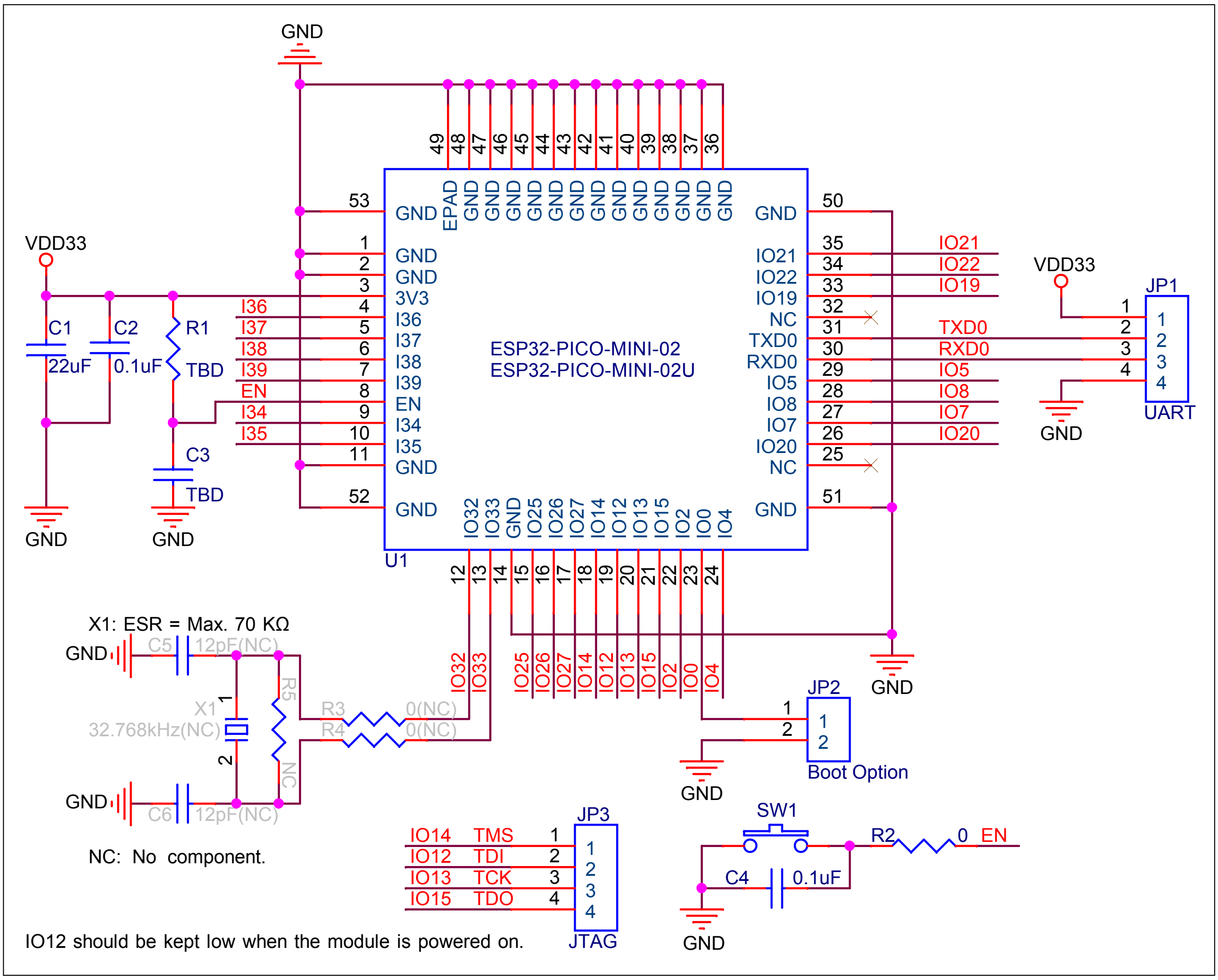


Figure 9: Peripheral Schematics

- Soldering EPAD Pin 49 to the ground of the base board is not a must. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As a result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32's power-up and reset sequence timing diagram, please refer to *ESP32 Series Datasheet* > Section *Power Supply*.
- UART0 is used to download firmware and log output. When using the AT firmware, please note that the UART GPIO is already configured (refer to *Hardware Connection*). It is recommended to use the default configuration.

10 Physical Dimensions

10.1 Module Dimensions

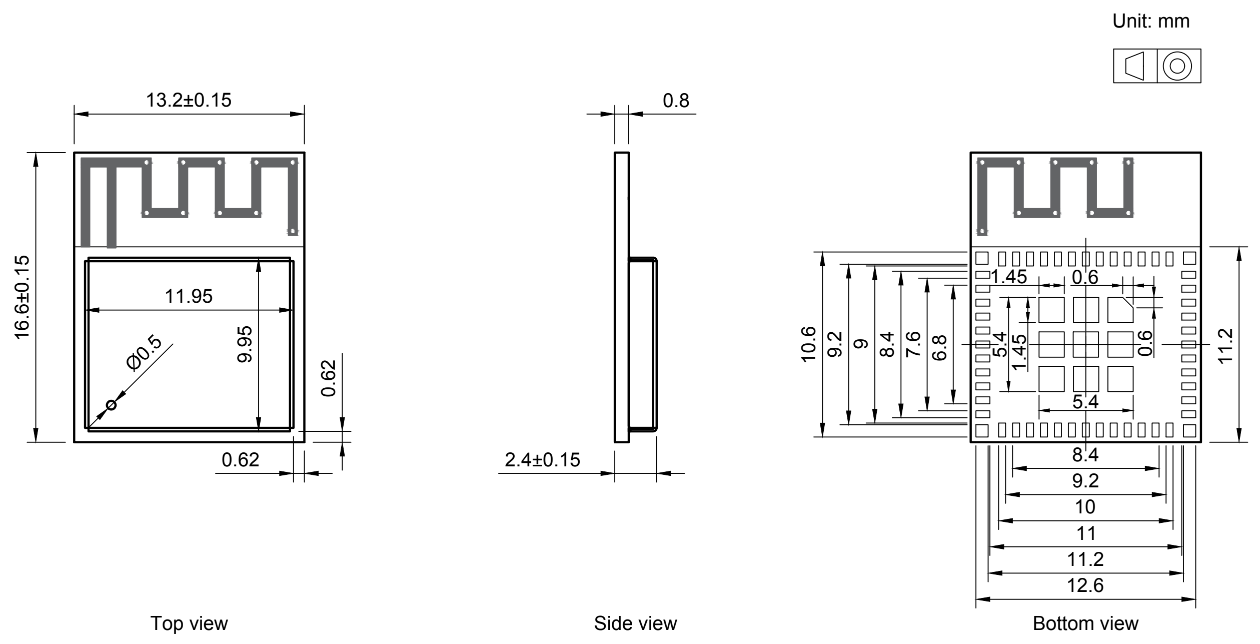


Figure 10: ESP32-PICO-MINI-02 Physical Dimensions

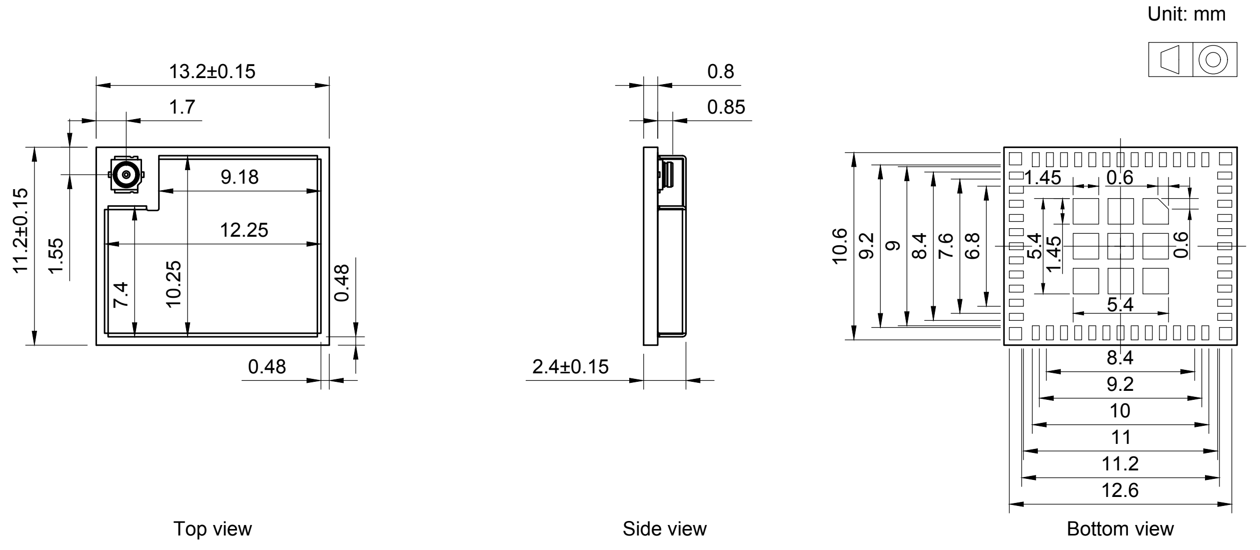


Figure 11: ESP32-PICO-MINI-02U Physical Dimensions

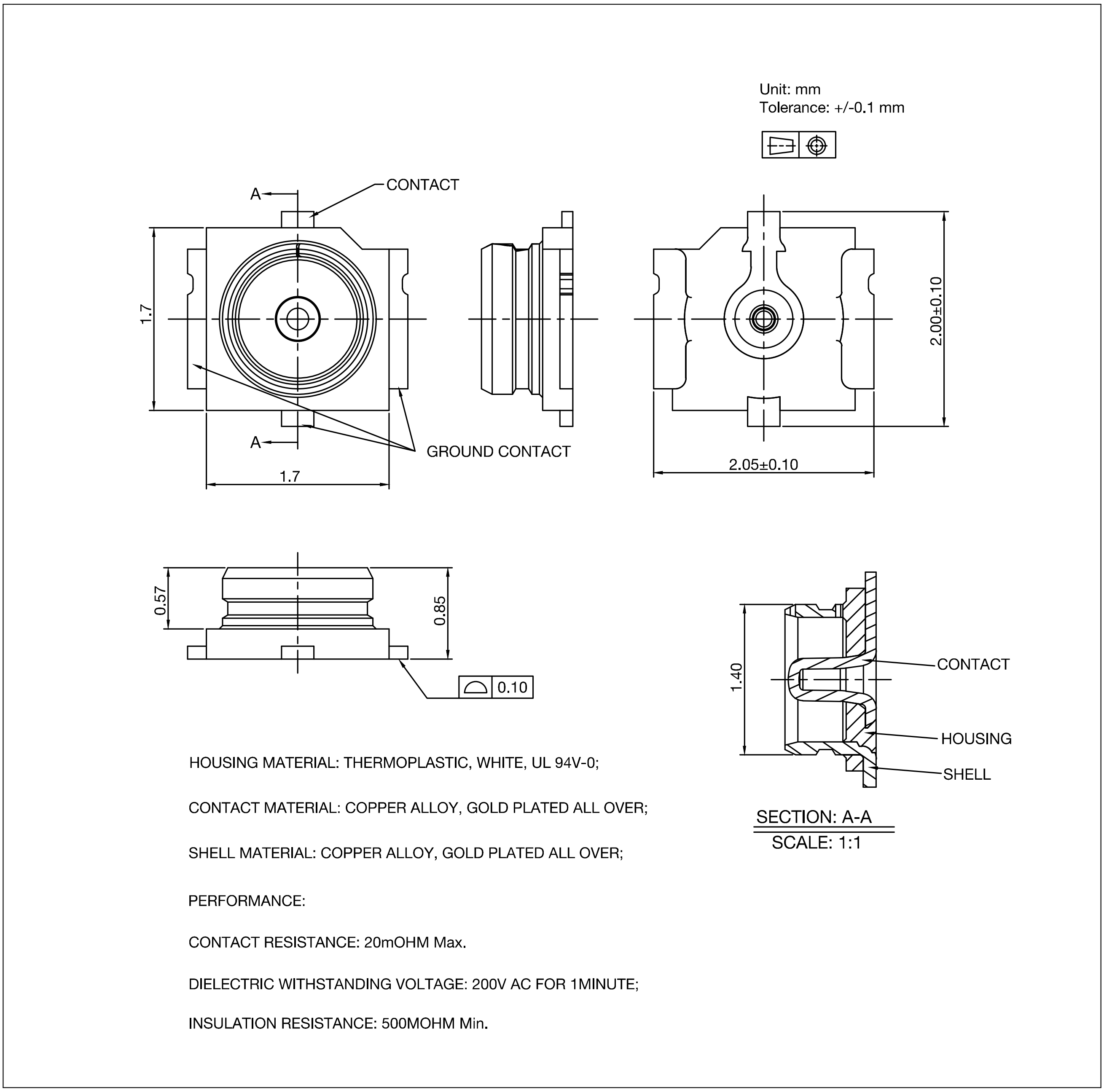
Note:

For information about tape, reel, and product marking, please refer to *Espressif Module Package Information*.

10.2 Dimensions of External Antenna Connector

ESP32-PICO-MINI-02U uses the third generation external antenna connector as shown in Figure 12. This connector is compatible with the following connectors:

- W.FL Series connector from Hirose
- MHF III connector from I-PEX
- AMMC connector from Amphenol



HOUSING MATERIAL: THERMOPLASTIC, WHITE, UL 94V-0;

CONTACT MATERIAL: COPPER ALLOY, GOLD PLATED ALL OVER;

SHELL MATERIAL: COPPER ALLOY, GOLD PLATED ALL OVER;

PERFORMANCE:

CONTACT RESISTANCE: 20mOHM Max.

DIELECTRIC WITHSTANDING VOLTAGE: 200V AC FOR 1MINUTE;

INSULATION RESISTANCE: 500MOHM Min.

Figure 12: Dimensions of External Antenna Connector

11 PCB Layout Recommendations

11.1 PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 13 *ESP32-PICO-MINI-02 Recommended PCB Land Pattern* and Figure 14 *ESP32-PICO-MINI-02U Recommended PCB Land Pattern*.
- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 13 and Figure 14. You can view the source files for ESP32-PICO-MINI-02 and ESP32-PICO-MINI-02U with Autodesk Viewer.

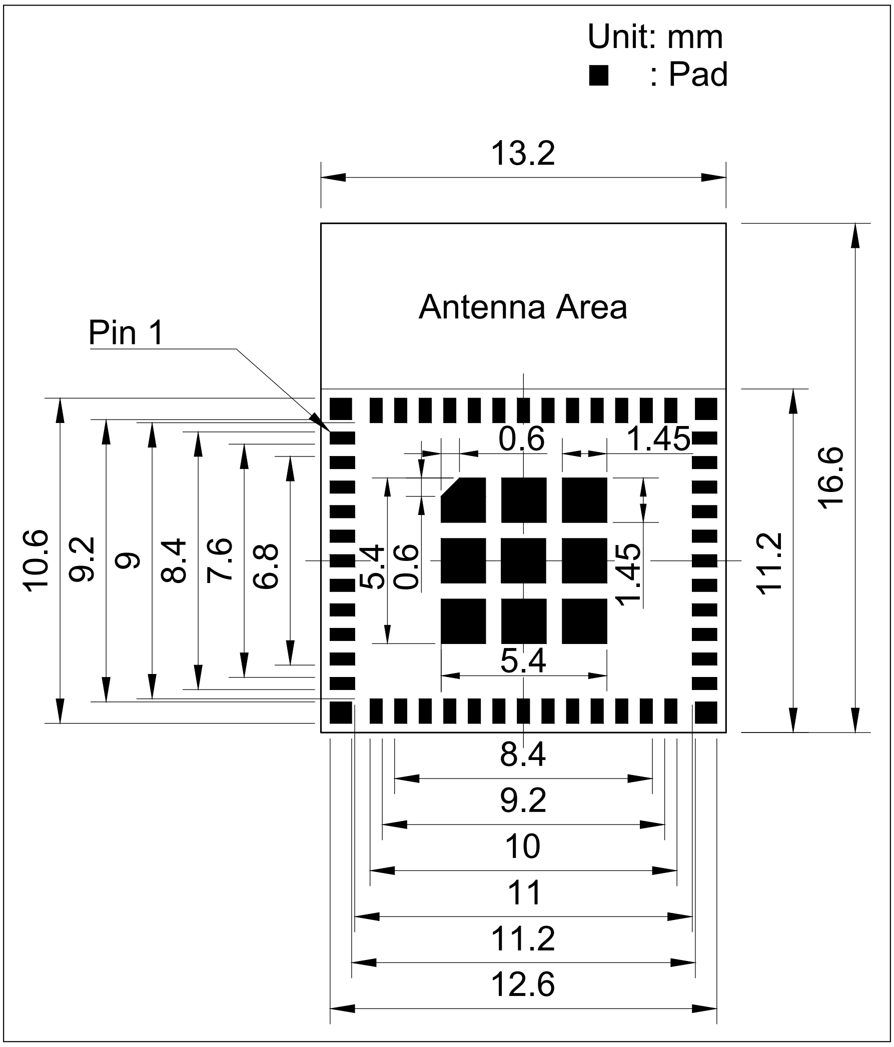


Figure 13: ESP32-PICO-MINI-02 Recommended PCB Land Pattern

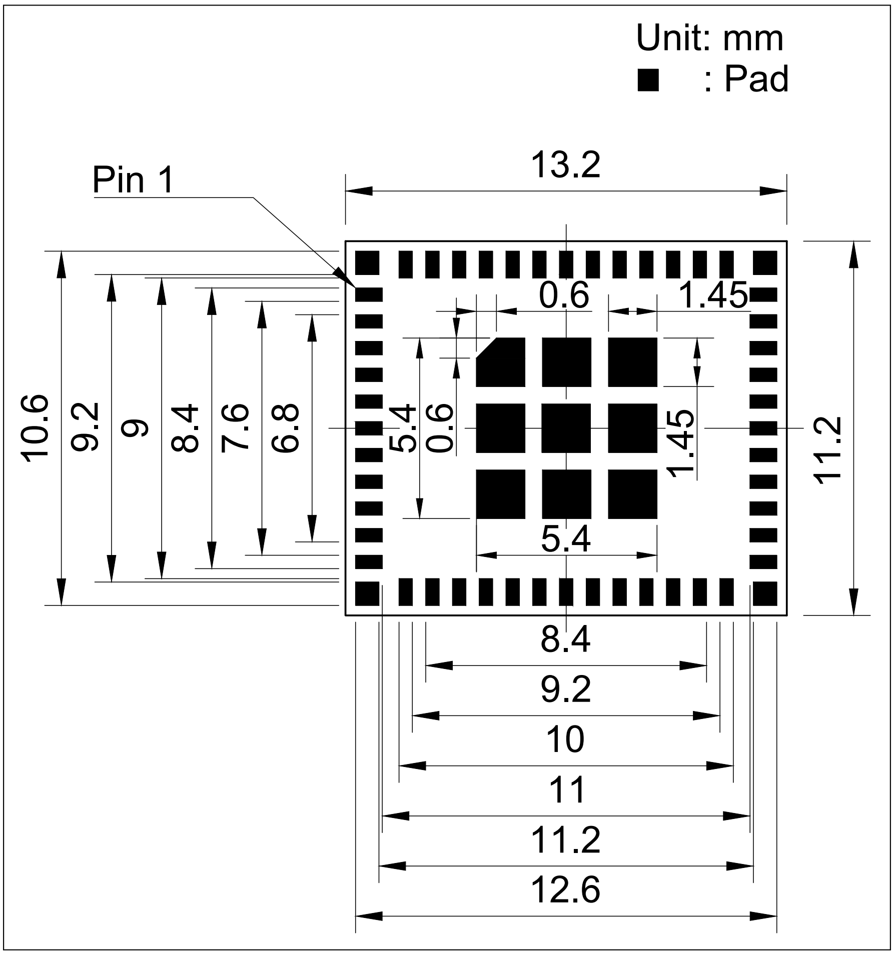


Figure 14: ESP32-PICO-MINI-02U Recommended PCB Land Pattern

11.2 Module Placement for PCB Design

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

For details about module placement for PCB design, please refer to *ESP32 Hardware Design Guidelines* > Section *Positioning a Module on a Base Board*.

12 Product Handling

12.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

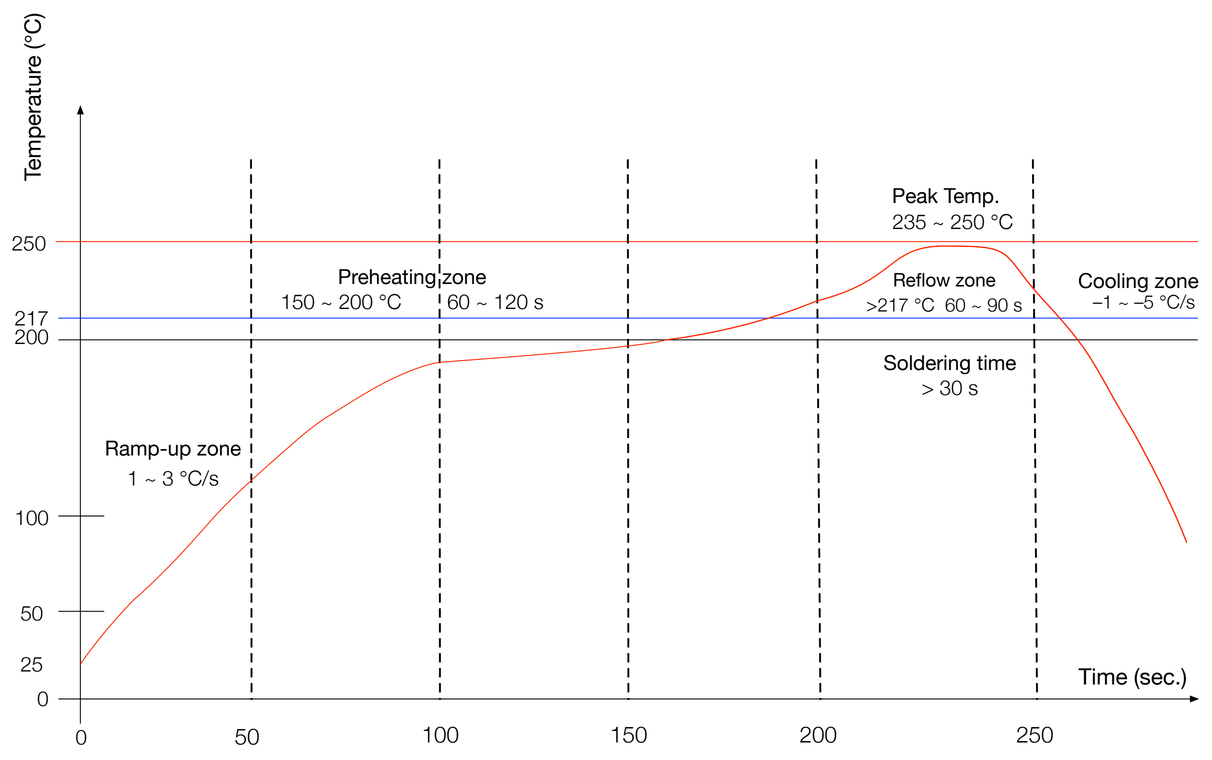
After unpacking, the module must be soldered within 168 hours with the factory conditions 25 ± 5 °C and 60 %RH. If the above conditions are not met, the module needs to be baked.

12.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

12.3 Reflow Profile

Solder the module in a single reflow.



Ramp-up zone — Temp.: 25 ~ 150 °C Time: 60 ~ 90 s Ramp-up rate: 1 ~ 3 °C/s
Preheating zone — Temp.: 150 ~ 200 °C Time: 60 ~ 120 s
Reflow zone — Temp.: >217 °C Time: 60 ~ 90 s; Peak Temp.: 235 ~ 250 °C Time: 30 ~ 70 s
Cooling zone — Peak Temp. ~ 180 °C Ramp-down rate: −1 ~ −5 °C/s
Solder — Sn-Ag-Cu (SAC305) lead-free solder alloy

Figure 15: Reflow Profile

12.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate.**

Related Documentation and Resources

Related Documentation

- ESP32 Series Datasheet – Specifications of the ESP32 hardware.
- ESP32 Technical Reference Manual – Detailed information on how to use the ESP32 memory and peripherals.
- ESP32 Hardware Design Guidelines – Guidelines on how to integrate the ESP32 into your hardware product.
- ESP32 ECO and Workarounds for Bugs – Correction of ESP32 design errors.
- ESP32 Series SoC Errata – Descriptions of known errors in ESP32 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns
- *ESP32 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32 Series SoCs* – Browse through all ESP32 SoCs.
  https://espressif.com/en/products/socs?id=ESP32
- *ESP32 Series Modules* – Browse through all ESP32-based modules.
  https://espressif.com/en/products/modules?id=ESP32
- *ESP32 Series DevKits* – Browse through all ESP32-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release notes
2025-03-19	v1.4	• Improved the wording and structure of following sections: – Updated Section *Features* and *Series Comparison* – Updated Section "Strapping Pins" and renamed to *Boot Configurations* – Added Chapter 5: *Peripherals* – Section 7: *RF Characteristics*: * Updated Table "Wi-Fi RF Standards" and renamed to *Wi-Fi RF Characteristics* * Added Table 19: *TX EVM Test* * Added Table 27: *Bluetooth LE RF Characteristics* – Section 9: *Peripheral Schematics*: Added a note about UART – Renamed Chapter "Physical Dimensions and PCB Land Pattern" to *Physical Dimensions* and added Chapter 11: *PCB Layout Recommendations*
2023-11-21	v1.3	Section 9: *Peripheral Schematics*: Updated the note about EPAD soldering under the figure Section 11.1: *PCB Land Pattern*: Added the modules' 2D PCB source files
2022-12-02	v1.2	Added Figure 5 and Table 5 in Section "Strapping Pins" that was renamed into *Boot Configurations* Added Section 12.4: *Ultrasonic Vibration*
2022-03-28	v1.1	Added a link to RF certificates in Section *Features* Updated the description of TWAI in Section *Features* Updated Table 13: *Recommended Operating Conditions*
2021-07-15	v1.0	Added ESP32-PICO-MINI-02U module. Updated the document formatting.
2021-03-16	v0.5	Preliminary release

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